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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/440,595	11/15/1999	NAVEED MAJID	PHA-23843	3147

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/440,595	Majid et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 2, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-7* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *4 and* ;
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida et al (US Pat. 6060748) in view of Oka et al (6140690), Takagi et al (US Pat. 6130458) and Lauffer et al (IDS-paper #4, European Pat. 0471938A1).

Regarding claim 1, Uchida et al disclose a multichip integrate circuit (IC) module (MCM)/device comprising:

-a high power semiconductor device (130, 130a and 130b in Fig. 1) such as MOS type field effect transistor (FET), bipolar transistor, etc. formed on a silicon-0n-insulator (SOI) substrate region (100 in Fig. 1; Col. 4, line 45- Col. 5, line 5) and a low power/low speed device (140 and 140a in Fig. 1) such as a transistor (Col. 5) formed on a silicon/bulk technology substrate region (120 in Fig. 1; Col. 5, line 16), and

- the high power and low power semiconductor devices/chips being directly mounted on a substrate (100/110/120, 200, 210, 11, etc. in Fig. 1-3)
(Fig. 1-3; Col. 4, line 45-Col. 7, line 10).

Uchida et al fail to specify the low power device/chip being a control chip and the power chip and control chip being directly mounted on the electrically conductive heat sink connected to ground potential.

Oka et al teach using a MCM where a power device (50 in Fig. 4 and 5) having a high voltage/current is disposed on a common substrate with a weak/low signal device (60 in Fig. 5) functioning as a control and a sensor device (Col. 2, line 15-25; Col. 5; Col. 17).

Lauffer et al teach using a multichip module having a variety of chips such as high power, low power, memory, logic chip, etc. comprising a bulk/conventional technology device and SOI device being directly mounted on the electrically conductive heat sink/substrate made of copper (11 in Fig. 4; Col. 9, line 7) which is connected to a ground potential (Col. 12, line 32).

Takagi et al teach using a multichip hybrid integrate circuit (IC)/module comprising a high/low level power semiconductor chips (200 in Fig. 12A and B) and respective high/low level control semiconductor chips (100 in Fig. 12A and B) devices

being directly mounted on an electrically conductive substrate connected to ground potential (81 in Fig. 12B; Col. 11, line 30-Col. 12, line 57).

The cited reference by Hill (US Pat. 6028348, Fig, 3; Col. 2, line 66) teach using a multichip module with the chips mounted on a conventional metal/electrically conductive substrate which serves as a heat sink.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a MCM having a power chip and a control chip being directly mounted on an electrically conductive heat sink substrate connected to ground potential so that heat dissipation and temperature distribution can be improved using Oka et al, Lauffer et al and Takagi et al's chip/substrate structures in Uchida et al's multichip module.

Regarding claims 2-4, Uchida et al fail to specify the control chip comprising BIMOS, CMOS or bipolar device.

Takagi et al disclose the control semiconductor chips comprising CMOS or any other conventional configurations comprising BICMOS, bipolar, n-MOS, etc. (Col. 13, line 64).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control chip comprising BIMOS, CMOS or bipolar device so that the current handling/breakdown voltage capability can be

improved Oka et al, Lauffer et al and Takagi et al's chip/substrate structures in Uchida et al's multichip module.

Regarding claims 5-7, the claim elements have been addressed as explained above in the rejection for claim 1.

Response to Arguments

2. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

09-12-02

Steven Loke